On the merits, the Office Action rejected Claims 1-20 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully believe that the amendment to Claim 1 adequately responds to the rejection. Withdrawal of the § 112, second paragraph rejection is respectfully requested.

Further on the merits, the Office Action rejected Claims 1-7 under 35 U.S.C. § 102(b) as being anticipated by Saran et al. (EP 0875934A2; hereinafter "Saran"). The Office Action also rejected Claim 2 under 35 U.S.C. § 103(a) as being obvious over Saran in view of Zavracky et al. (U.S. Patent No. 5,796,953; hereinafter "Zavracky"). Applicants respectfully submit that the pending claims are patentable for at least the following reasons:

Applicants' claim 1 recites: "A semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, wherein the layered structure comprises a metal layer and a layer of a dielectric material, characterized in that via lines are present in the layer of dielectric material, which via lines are arranged in such a way that the metal layers and the via lines form all isolated areas filled with the dielectric material."

As stated in Applicants' specification on page 2, lines 18-34, Sarma recites only forming vias on the pad periphery. This leads to cracking of the dielectric layer due to bonding or probing. Sarma fails to recite or suggest the metal layers and the via lines form all isolated areas filled with the dielectric material. Consequently, Sarma fails to recite or suggest all the claimed limitations of Claim 1. Claim 1 is believed patentable for at least these reasons.

Claims 2-7 depend from Claim 1 and are believed patentable for at least the same reasons. In addition, In addition, Applicants respectfully believe Claims 2-7 to be independently patentable and request separate consideration of each claim. Further, Applicants believe the § 103 rejections of Claim 2 to be moot in light of the above amendments and remarks. Consequently, withdrawal of the § 103 rejections is respectfully requested.

In view of the foregoing remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned agent may be reached by telephone at the number given below.

Respectfully submitted,

By _____

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APPENDIX A
MARKED-UP CLAIMS

1. (Amended) A semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure~~, but preferably a stack of layered structures~~, wherein the layered structure comprises a metal layer and a layer of a dielectric material, characterized in that via lines are present in the layer of dielectric material, which via lines are arranged in such a way that the metal layers and the via lines form all isolated areas filled with the dielectric material.

APPEDIX B
MARKED-UP SPECIFICATION

Semiconductor device

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor devices and more specifically to integrated circuits (ICs) having bond pads incorporated therein. More particularly, the invention relates to a semiconductor device comprising a new bond pad structure wherein cracking is eliminated, or at least reduced. More in detail, the present invention relates to a semiconductor device comprising a bond pad structure, which enables wire bonding and probing to be carried out without the induction of - or at least with a reduced occurrence of - cracks in the intermetal dielectrics applied.

BACKGROUND OF THE INVENTION

In state-of-the-art IC technology, bond pads consist of a multilayer aluminum metallization, generally with one or more layers of e.g. titanium or titanium nitride. Bond pads are present for attaching solder, wire or other bonding elements, especially constructed from aluminum, gold or copper.

Bond pads are typically disposed above one or more layers or stacks of brittle and/or soft intermetal dielectric materials, such as silicon oxides and organic materials.

Bond pad cracks can occur during ultrasonic wire bonding or even through probing. Cracks can lead to reliability problems, especially when low-k spin-on dielectrics, such as hydrogen silsesquioxane (HSQ), are used. Such dielectrics, and especially HSQ, are more brittle than other oxides, such as tetraethoxysilane-based oxides. In HSQ layers cracks can therefore more easily propagate than in other oxides. Similar problems occur with aerogels, organic polyimides, parylenes and the like, which all have low dielectric constants as compared to silicon oxides, but are structurally and mechanically weaker than these oxides.

In the art, there is a need for structures or methods to prevent or at least reduce the occurrence of bond pad cracking.

It has been proposed in EP-A-0 875 934 to dispose a patterned reinforcing structure in a dielectric layer disposed under the bond pad. The basic principle laid down in this document is that through the use of metal grids mechanical reinforcement of the dielectric stack can be achieved and damage due to bonding can be prevented. More in detail, this known reinforced structure is manufactured by forming a metal layer, patterning the metal layer in a predetermined area in accordance with a predetermined pattern having a plurality of vacant areas, forming a dielectric layer above the patterned metal layer, and filling the vacant areas in the patterned metal layer. Finally, a bond pad is formed on the dielectric layer above the patterned metal layer.

The known reinforcing structure may be a joined or interconnected grid or a crosshatch structure with a plurality of voids or vacant areas for containing and accommodating a large portion of weak dielectric material such as the said HSQ and the like. The grid structure is planar with a thickness below the thickness of the intermetal dielectric stack. In another embodiment, the reinforcing structure includes a repeating and non-interconnected pattern such as a crucifix pattern arranged in a regular manner. Other structures such as spirals have been described as well.

The present inventors have intensively studied two of the structures known from EP-A-0 875 934:

- the crosshatch structure, wherein at each metal level, under the bond pad, a crosshatch grid of metal was inserted to confine mechanically relatively weak HSQ into square reservoirs created by the grid; and
- the crucifix structure. This structure provides a more open metal pattern as compared with the crosshatch structure, allowing HSQ to flow more easily into the voids.

In the crosshatch structure, the metal line widths and spacings were designed to confine much of the HSQ into the reservoirs while minimizing the area of each reservoir, so that the HSQ layer is spared the direct mechanical impact of bonding. Vias were formed only at the pad periphery.

In the crucifix structure, the more open pattern allows the HSQ to flow more easily in the voids present in the structure. By virtue thereof, the amount of HSQ remaining over the metal lines is reduced slightly further as compared to the crosshatch structure.

Both known structures have, however, a continuous TEOS dielectric layer between the metal layers, which dielectric layer can be cracked due to bonding or probing.

SUMMARY OF THE INVENTION

The present invention aims to solve or at least reduce this problem.

In accordance with the present invention, it has now been found that elimination, or at least reduction of bond pad cracking can be achieved by isolating the intermetal dielectrics with metal lines and via lines. Further, the bond pad structure of the semiconductor device according to the present invention prevents the propagation of any cracks that are formed. Moreover, metal peel off during bonding is diminished. Metal peel off is a failure mode occurring at the interface between a top metal plate and intermetal dielectrics.

More in detail, the present invention is based on the principle that use is made of via lines together with metal lines to completely isolate intermetal dielectrics. For this purpose, the invention relates to a semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material, characterized in that via lines are present in the layer of dielectric material, which via lines are arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

Furthermore, the present invention relates to a method of manufacturing a semiconductor device as described above, which method comprises the steps of:

(a) forming a metal layer;

(b) forming a dielectric layer;

(c) patterning via lines or via grids in the dielectric layer;

(d) filling the patterned via lines or via grids with a conductive material, such as a metal, and preferably tungsten or copper; and

(e) applying a metal bond pad on top of the dielectric layer and the filled via lines or via grids.

By the use of via lines connected to the metal layer, the adhesion between the top metal plate and the underlying layers is enhanced, so that metal peal off occurs no longer or less often.

Without being bound by a very specific theory, it is assumed that when a crack is formed in an intermetal dielectric, the system releases elastic energy and gains surface energy. Based on thermodynamic principles, the crack should not form when the amount of elastic energy to be released is smaller than the amount of surface energy to be gained. Since elastic energy is proportional to the volume of the dielectric and surface energy is proportional to the surface area of the dielectric, the present invention makes use of a small volume-to-area ratio by using small feature sizes. Therefore, the via lines, or optionally the via grids, are advantageously arranged in such a way that the volume-to-surface area is - dependent on the dielectric material used - adjusted such that the amount of elastic energy to be released when a crack is formed is smaller than the amount of surface energy to be gained when said crack is formed.

Apart from the above, it is noted that in the art vias are normally patterned in square or round pillars. Multiple rows of such pillars, shifted with respect to each other, are in use in e.g. seal rings to prevent the propagation of cracks. However, in accordance with the present invention, via lines, e.g. in the form of a via grid, avoid the formation of cracks as well as the propagation in case a crack is formed anyway. Moreover, bonding stress can be released by ductile properties of the via-metal, in particular when tungsten is used as the via-metal.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be described in further detail with reference to the drawings, wherein

Fig. 1 is a schematic top view of the bond pad structure of the semiconductor device according to the invention;

Figs. 2 and 3 are cross-sections of two embodiments of the bond pad structure of the semiconductor device of the present invention, wherein the upper cross-sections of Figs. 2 and 3 are cross-sections of the structure of Fig. 1 indicated by means of the upper arrow, while the lower cross-sections of Figs. 2 and 3 are cross-sections of the structure of Fig. 1 indicated by means of the lower arrow.

DETAILED DESCRIPTION OF THE PRIMARY EMBODIMENT

Fig. 1 shows a schematic top view of the bond pad structure of the semiconductor device of the present invention at via level. This top view shows the crosshatch feature of the structures. Intermetal dielectrics are isolated by metal and via lines. The details will become clear from Figs. 2 and 3.

In Fig. 2, an embodiment is shown wherein each layered structure comprises a metal plate 1. Intermetal dielectrics 4 are isolated by two adjacent metal plates 1 and, in the vertical direction, by via lines or via grids 3.

Fig. 3 shows the embodiment wherein the top and bottom layered structures comprise a metal plate 1, while the intermediate layered structures are formed by metal lines or metal grids 2. Intermetal dielectrics 4 are isolated by the top and bottom metal plates 1 and by the metal lines or metal grids 2 and via lines or via grids 3 in between.

The distances between the via lines or via grids in a particular layer structure are chosen to be such that the volume-to-surface area ratio of the dielectrics 4 in the direction parallel to the bond pad is sufficiently small to prevent crack formation during probing or bonding. For example, when the dielectrics thickness is 1 μm, the width and length of the dielectric block should be smaller than 10 μm. Normally, a bond pad size is about 80 x 80 μm. Without the isolation of the dielectric layers cracks can easily form.

On top of the structures in accordance with the invention a bond pad, preferably of Al, is applied.

ABSTRACT:

The invention relates to a semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material. In the layer of dielectric material via lines are present and arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

~~Fig. 3~~